stream to a first input **31** of a downstream mixer **33**, which multiplies the "long" code sequence by a "short", multichip sequence to produce a composite sequence that is applied to a downstream RF modulator (not shown) for transmission. By "long" spreading sequence is meant that the period or duration of the "long" code sequence is considerably longer (e.g. an order of magnitude or more) than the "short" spreading sequence produced by a "short" spreading sequence generator **35**, the output of which is coupled to a second input **37** of mixer **33**. In addition, the length of the "long" spreading sequence is equal to or longer than the period of a data bit.

More particularly, as illustrated in FIG. **2**, which shows the timing relationships among the data and the two ("long" and "short") spreading sequences, in the course of the BPSK encoding process, each bit period Tb of the data is effectively subdivided into a plurality of M (eight in the present example) "short" intervals Ts. Using a 16 kbps data rate as an illustrative example, each short interval Ts has a duration on the order of 62.5/8=7.813 microseconds. The "short" spreading sequence produced by generator **35** is comprised of a sequence of N pseudo random spreading chips, e.g. **127** chips per interval Ts, which is multiplied by each of the bits of the first spread modulation output bit stream produced by mixer **21**, so that during each bit interval Tb, mixer **21** produces NXM (8X127=1016) chips. In accordance with the present invention, the length of the "long" spreading sequence is fractionally longer than the bit period Tb, e.g. seven-eighths of a bit time longer than a data bit, so that the duration of the "long" sequence is fifteen times the duration of the "short" sequence. As a result, the "long" spreading sequence repeats at intervals that are incrementally offset, or delayed, by the length of a "short" sequence for successive bit periods Tb, so that the bits of the "long" sequence occur at different times for successive data bits. Consequently, the composite, or compound, sequence produced by mixer **33** has reduced spectral ripple and does not produce spectral lines that are exhibited by a repetitive short code alone. In addition, because the bit period Tb (eight "short" code intervals Ts) and the length (15Ts) of the relatively "long" coding sequence are relatively prime, bit starts will occur at all chips of the "long" code with equal frequency, so that the auto correlation function of the long code may be considered approximately implied on the autocorrelation function of the composite spread signal.

Referring now to FIG. **3**, an embodiment of a demodulator for despreading and decoding the composite code produced by the output of mixer **33** in the transmitter terminal unit of FIG. **1** is diagrammatically illustrated as comprising an IF input line **41**, over which a composite signal from an associated RF downconverter of the receiver terminal is coupled. As explained above, the design of the demodulator takes advantage of the fact that the relatively "short" sequence (one-eighth of a bit time) within the received composite code can be despread using a practical-sized passive device. In accordance with a preferred embodiment of the invention, despreading of the "short" sequence is accomplished by applying the composite spread signal on link **41** to a conventional surface acoustic wave matched filter **43**, the electrode pattern of which effectively corresponds to the **127** chip sequence of the "short" code and thereby produces over an output line **45** a first despread signal comprised of the product of the "long" sequence and the BPSK-encoded data. The output of matched filter **43** is fed to a first input **47** of a mixer **51**, which combines the first despread output signal with a replica of the "long" coding sequence produced by a "long" code generator **53**, the output of which is coupled to a second input **55** of mixer **51**. Long code generator is driven by a local pseudo noise clock signal on clock link **57** and is controlled by the receiver's control processor **61**. Mixer **51** produces a second despread output signal on output line **59**, corresponding to the BPSK encoded data absent both the "long" and the "short" sequences of the composite code, and couples the despread signal to a DPSK decoder **63**, comprised of multiplier **65** and an associated delay line **67**. Like matched filter **43**, delay line **67** is preferably implemented as an SAW device, in order to simplify the hardware. Its delay period corresponds to the subdivision of the bit period used in the differential PSK encoding process at the transmitter which, in the present example, is one-eighth of a bit period (i.e. Tb/8). The output of multiplier **65** is a series of positive or negative pulses corresponding to the channel multipath response which repeats at a periodic rate equal to the long code chip rate (eight times the bit rate).

These decoded output pulses are coupled to an integrate and dump circuit **71**, diagrammatically illustrated in FIG. **3** as a cascaded gate, or switch, **73** and an integrator **75**, which gates and integrates the pulses over the eight long code chips of a bit so as to perform combining of the multipath energy. The output of integrator **75** is coupled to a hard-limiter **81**, which makes a data bit decision by comparing the accumulated contents with a reference value (zero). Thus the data bit is determined to be a "0" if the energy is less than the reference, and a "1" if the accumulated energy is greater than the reference. After each bit decision, the contents of integrator **75** are cleared or dumped.

As pointed out previously, and as will be appreciated from the foregoing description, simplification of the hardware configuration of a spread spectrum demodulator is obtained in accordance with the present invention by the use of a composite spreading mechanism that permits part of the signal despreading process to be carried out by means of a practical sized, passive matched filter, thereby reducing processing complexity and power consumption. The digital hardware intensity of the demodulator may be further reduced by using analog components for other portions of the signal processor, such as mixer **51** which performs a despread multiply function, an SAW structure for delay line **67** employed in the DCPSK decoder and by using RC components for the integrate and dump circuit.

While we have shown and described an embodiment in accordance with the present invention, it is to be understood that the same is not limited thereto but is suspectible to numerous changes and modifications as known to a person skilled in the art, and we therefore do not wish to be limited to the details shown and described herein but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.

We claim:

1. An apparatus for demodulating modulated information signals that are comprised of information signals that have been combined with a first code sequence and with a second code sequence, said second code sequence being shorter than said first code sequence, to produce modulated information signals comprising: